Loadless 4T SRAM cell with PMOS drivers

ABSTRACT

The instant invention comprises a memory cell with PMOS drive transistors (170, 180) and NMOS pass transistors (150, 160). A NMOS transistor is connected between a storage node (230) and a bitline (200). The NMOS transistor is gated by the wordline (190). A PMOS drive transistor (180) is connected between the storage node (230) and a supply voltage (255).